AMENDMENTS TO THE CLAIMS

The listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1. (previously presented) A method for generating a semiconductor structure, comprising:

a buried first semiconductor layer of a first doping type;

a second semiconductor layer of the first doping type on the buried semiconductor layer, which is less doped than the buried first semiconductor layer;

a semiconductor area of a second doping type on the second semiconductor layer, so that a pn junction is formed between the semiconductor area and the second semiconductor layer; and

a recess present below the semiconductor area in the buried first semiconductor layer, which contains a further semiconductor area of the first doping type, which lies deeper in the substrate than the buried first semiconductor layer, such that the breakdown voltage across the pn junction is higher than if the recess were not provided

the method comprising,

providing the buried first semiconductor layer with the recess formed therein,

performing an implantation for introducing a doping of the first doping type into the recess to generate the further semiconductor area of the first doping type, which lies deeper in the substrate than the buried first layer;

generating the second semiconductor layer on the buried first semiconductor layer, which is less doped than the buried first semiconductor layer, prior to or after performing the implantation; and

generating the semiconductor area of the second doping type on the second semiconductor layer in order to form the pn junction.

Claim 2. (canceled)

Claim 3. (currently amended) The method according to claim ~~2~~ 1, wherein the further semiconductor area is doped equal or less than the buried first semiconductor layer.

Claim 4. (canceled)

Claim 5. (previously presented) The method according to claim 1, wherein the semiconductor area is a base, the first buried semiconductor layer a subcollector and the second semiconductor layer a collector of a bipolar transistor.

Claim 6. (withdrawn) Semiconductor structure according to claim 5, wherein a portion of the buried first semiconductor layer further represents a subcollector for at least another bipolar transistor, wherein the recess is not formed in the portion of the buried first semiconductor layer for the at least another bipolar transistor and the bipolar transistor and the at least another bipolar transistor have different breakdown voltages.

Claim 7. (currently amended) The method according to claim 1, wherein a portion of the first buried semiconductor layer is formed to include a second recess configured for another bipolar transistor, and wherein the buried first semiconductor layer has recesses of different widths for the bipolar transistors.

Claim 8. (canceled)

Claim 9. (previously presented) The method according to claim 1, wherein the step of providing comprises:

depositing an implantation mask on a semiconductor substrate, wherein the implantation mask covers the recess;

implanting the buried first semiconductor layer by using the implantation mask.

Claim 10. (previously presented) The method according to claim 9, further comprising:

depositing a further implantation mask, which leaves the recess exposed, after the step of providing; and

generating the further semiconductor area in the recess by using the further implantation mask.

Claim 11. (canceled)

Claim 12. (previously presented) A method comprising the steps of:

providing spaced apart first and second buried first semiconductor layers of a first doping type and a first doping value buried in a substrate, the first buried first semiconductor layer being formed to include a recess therein and acting as a region of a first bipolar transistor, the second buried first semiconductor layer acting as a region of a second bipolar transistor;

introducing a further semiconductor area of the first doping type in the recess, wherein after the introducing step, the further semiconductor material lies deeper in the substrate than the first buried first semiconductor layer;

generating a second semiconductor layer of the first doping type on each of the first and second buried first semiconductor layers;

generating a semiconductor area of a second doping type on each of the second semiconductor layers to form pn junctions;

wherein the breakdown voltage across the pn junction of the first bipolar transistor is higher than if the recess were not present; and,

wherein the first and second buried first semiconductor layers are provided during a single doping step.

Claim 13. (previously presented) The method of claim 12 wherein the doping of the further semiconductor layer is higher than the doping of the second semiconductor layer.

Claim 14. (previously presented) The method of claim 13 wherein the doping of the further semiconductor layer is not higher than the doping of the first buried first semiconductor layer.

Claim 15. (previously presented) The method of claim 14 wherein the generating a second semiconductor layer step includes generating a portion of the second semiconductor layer so that it extends into the recess.

Claim 16. (previously presented) The method of claim 15 wherein the second bipolar transistor has a different breakdown voltage than the first bipolar transistor.

Claim 17. (withdrawn) The method of claim 16 wherein the provided second buried first semiconductor layer contains no recess.

Claim 18. (previously presented) The method of claim 16 wherein the provided second buried semiconductor layer is formed to include a recess having a different width than the recess in the provided first buried first semiconductor layer.

Claim 19. (previously presented) The method of claim 16 wherein the first buried first semiconductor layer is a subcollector of the first bipolar transistor.

Claim 20. (previously presented) The method of claim 19 wherein the second first buried semiconductor layer is a subcollector of the second bipolar transistor.